MICRO-428: Metrology

Week Eleven: Electrical Metrology

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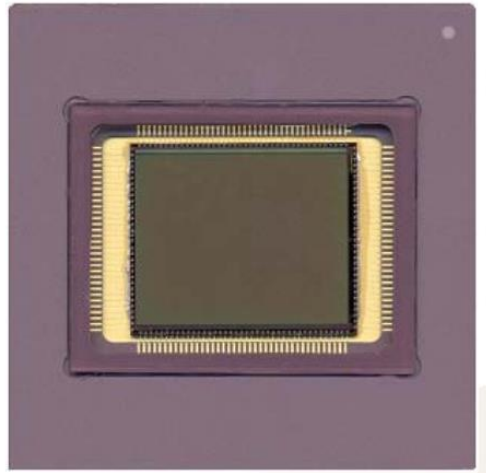
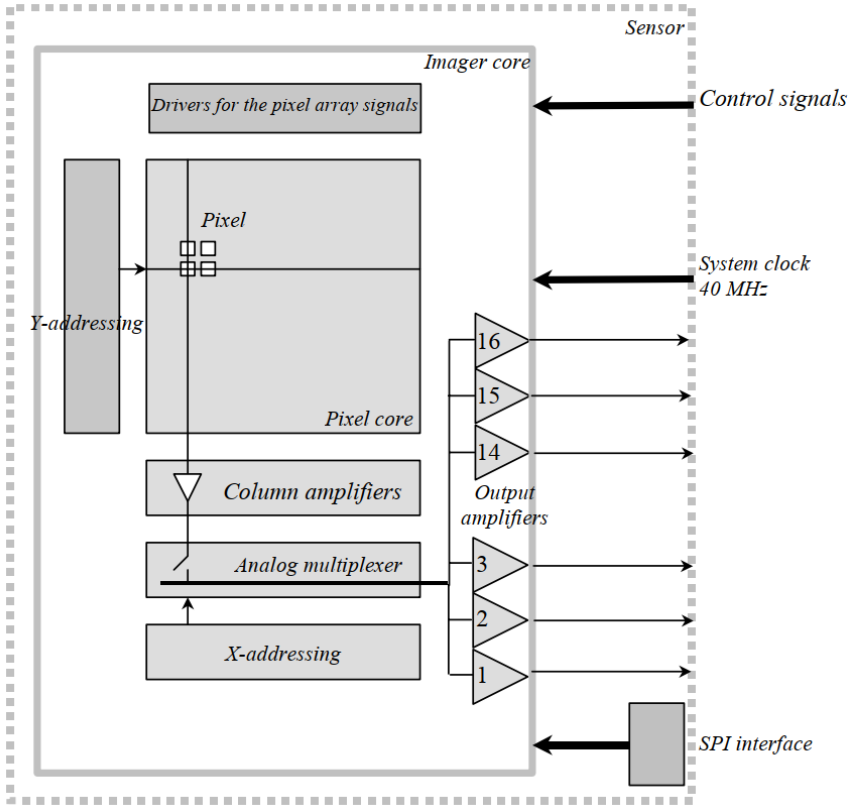
Exercise 1: Video digitization

- The objective is to determine the appropriate ADC to utilize in a cell phone camera alongside a CMOS array. An instance of a high-speed CMOS sensing chip is the LUPA-1300 from Cypress Electronics





Relevant information derived from the specifications are:

- **1280×1024** pixels, each **14 µm square**.
- Full well capacity: **62500** electrons.
- Output at **60,000** electrons: **1 V**.
- Typical quantum efficiency across the visible spectrum: **15%**.
- Dark current and read noise: **45 e^-/pixel**
- Recommended clock speed (pixel read rate): **40 MHz**

Output read by **16 parallel amplifier** channels (so each channel only looks at **an 80×1024 subarray**).

📖 https://www.asdlib.org/onlineArticles/elabware/Scheeline_ADC/

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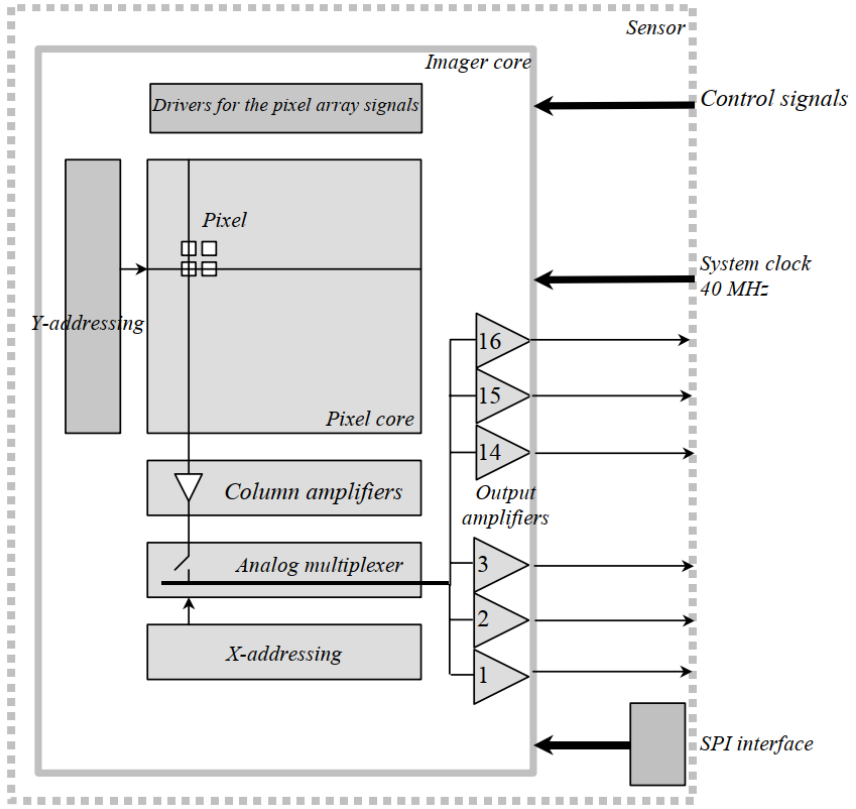

1/ What is the appropriate number of bits for resolution?

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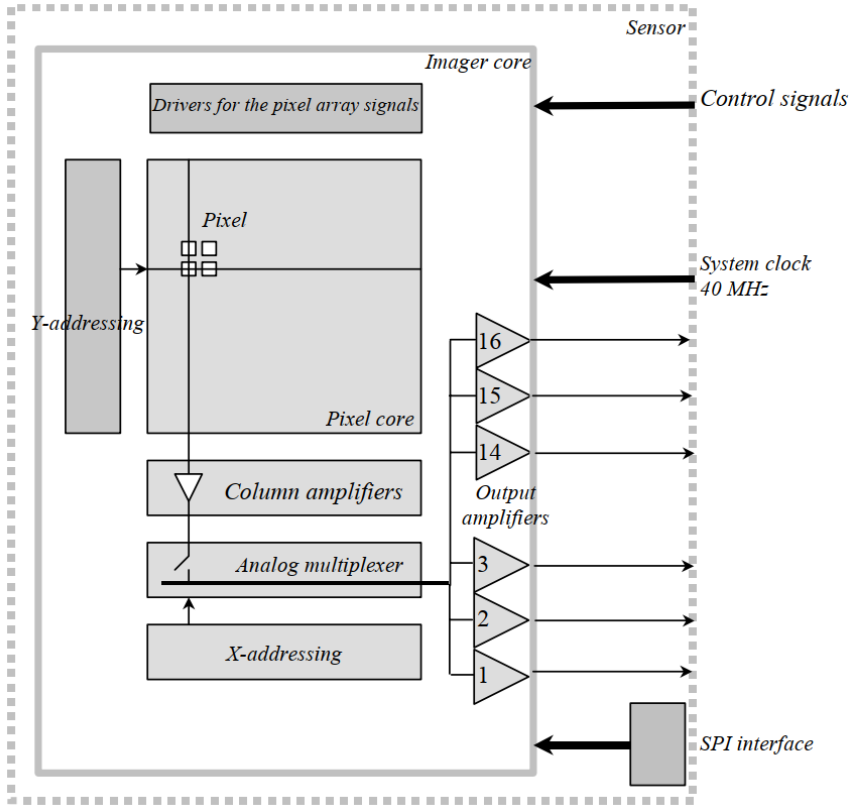

1/ What is the appropriate number of bits for resolution?

Maximum limit: Full scale is 62500 electrons, so even if there were no noise, the biggest useful number would be just short of 65536 = 2^{16}.

Minimum limit: The dark current and read noise come to 45 e^-, the shot noise limit is thus $\sqrt{45}\ e^-$, meaning that each digitization has an uncertainty of 6-7 electrons => The highest useful count is: 62500/6 = 10411 counts, that's between 2^{13} and 2^{14}.

Choosing 1 bit amplitude = 7 electrons, then the appropriate number of bits for the ADC are **14 bits**.

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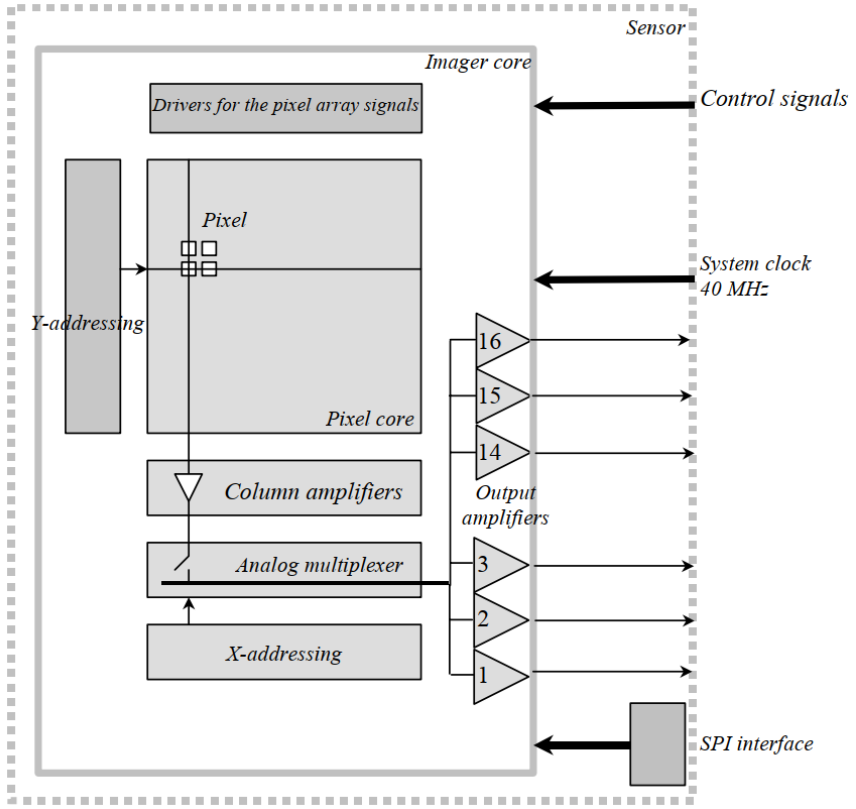

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Hint: Each ADC is dedicated to a single channel. The problem specifies the conversion rate per channel, which makes it possible to calculate the number of pixels associated with that particular channel.

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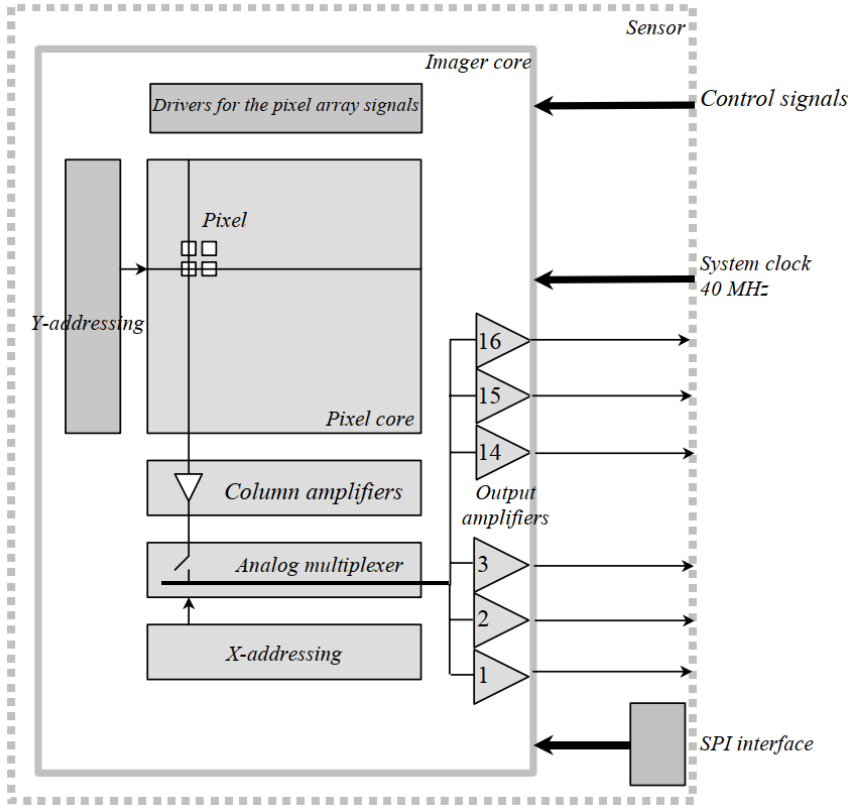

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Considering that the optimal clocking speed of the array is **40 MHz**, each channel must perform digitization at the same speed. Each channel is responsible for analyzing **80 × 1024 pixels**, which corresponds to **81920 pixels**. Consequently, we can digitize the output of the array at a frequency of $4 \times 10^7 / 81920 = 488$ Hz.

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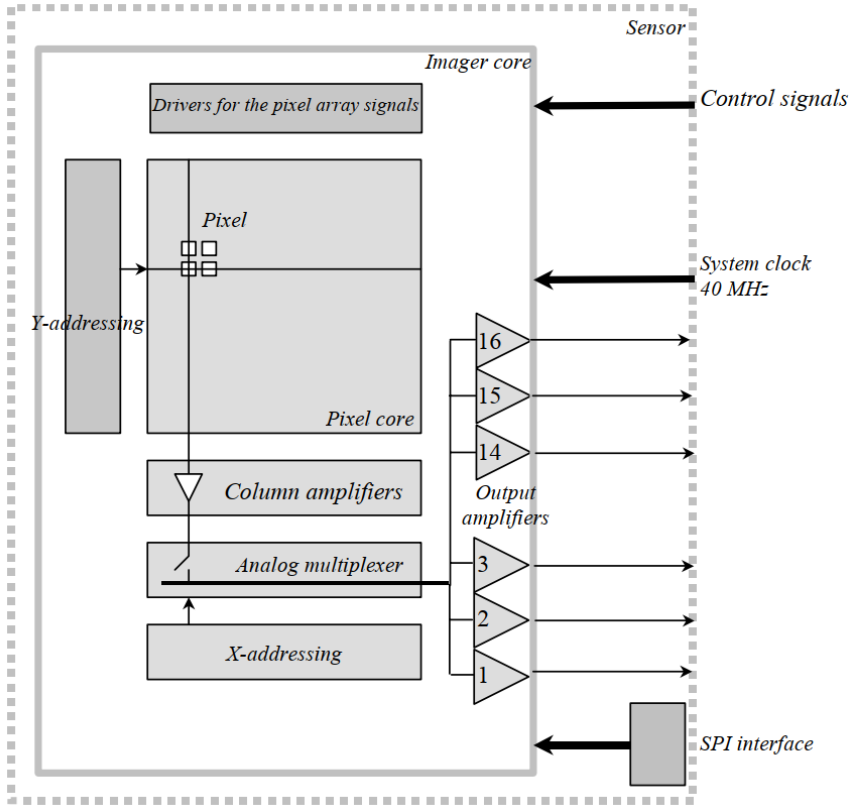
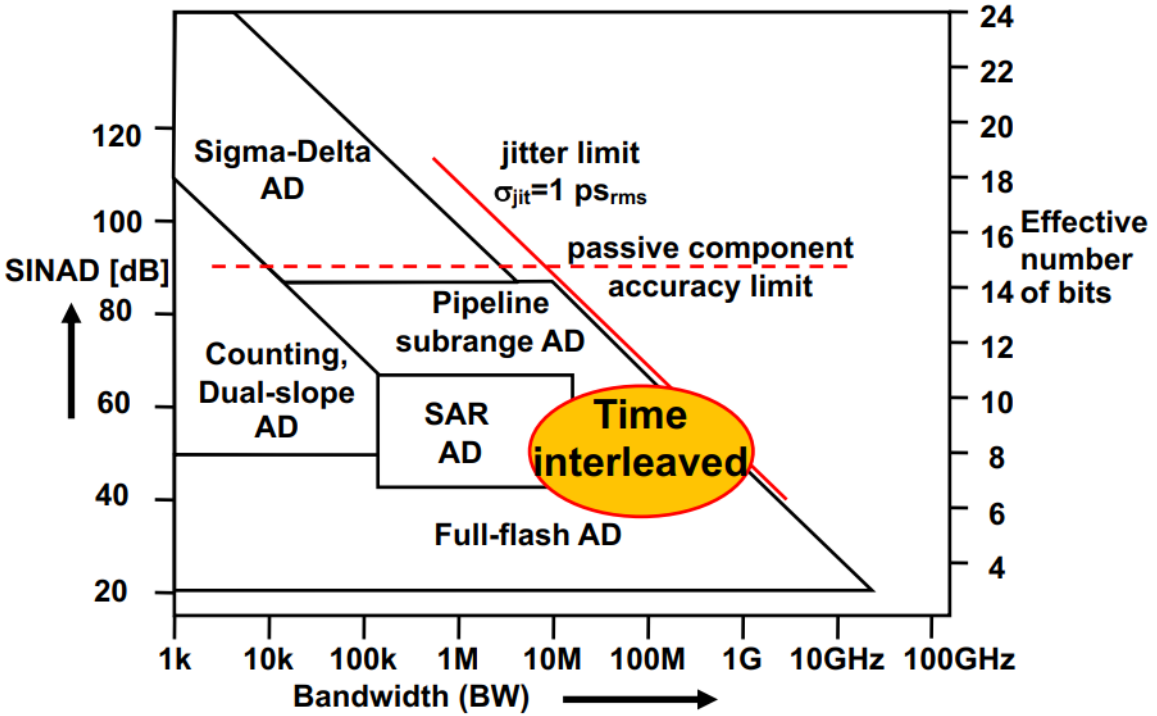
3/ Which ADC type would you suggest using?





Mead courses, “Data converters”, 2021

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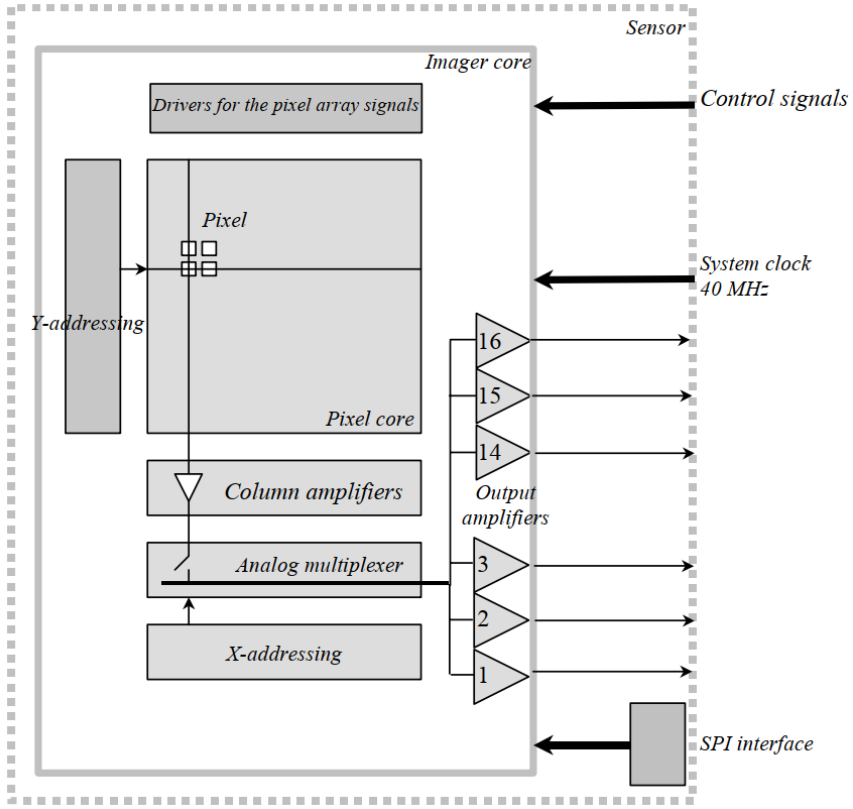
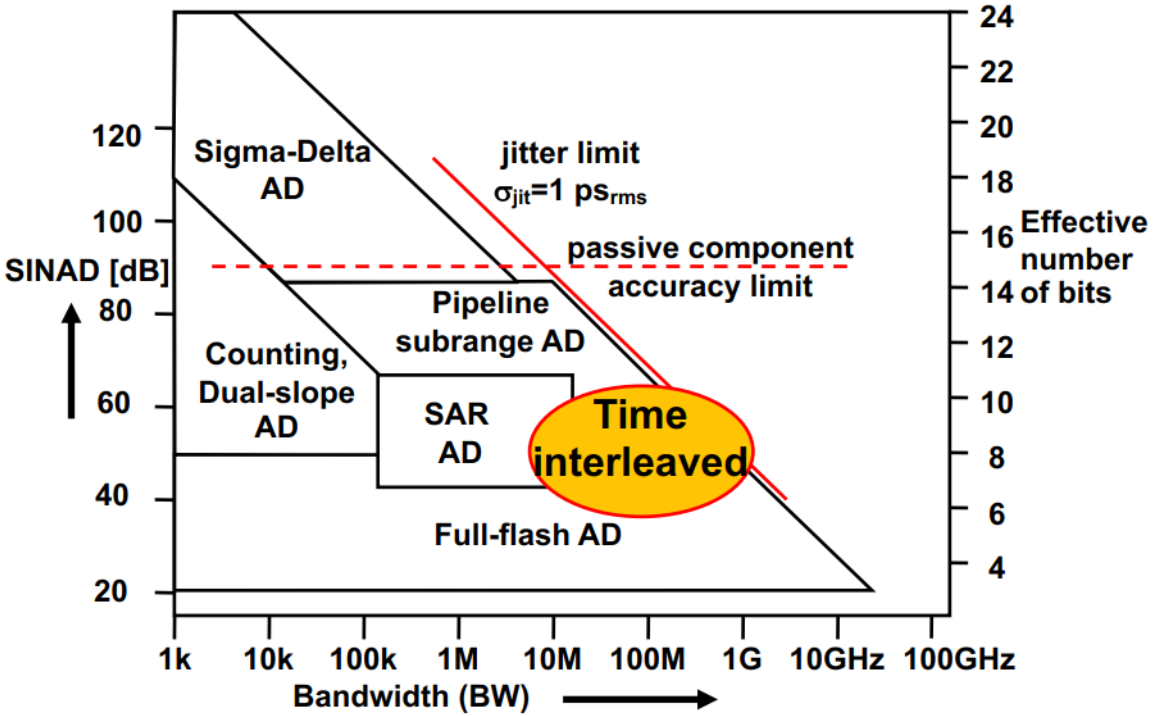


Mead courses, "Data converters", 2021

3/ Which ADC type would you suggest using?

We must either use a 14-bit ADC that can function at a speed of 40 MHz, or reduce the output rate.



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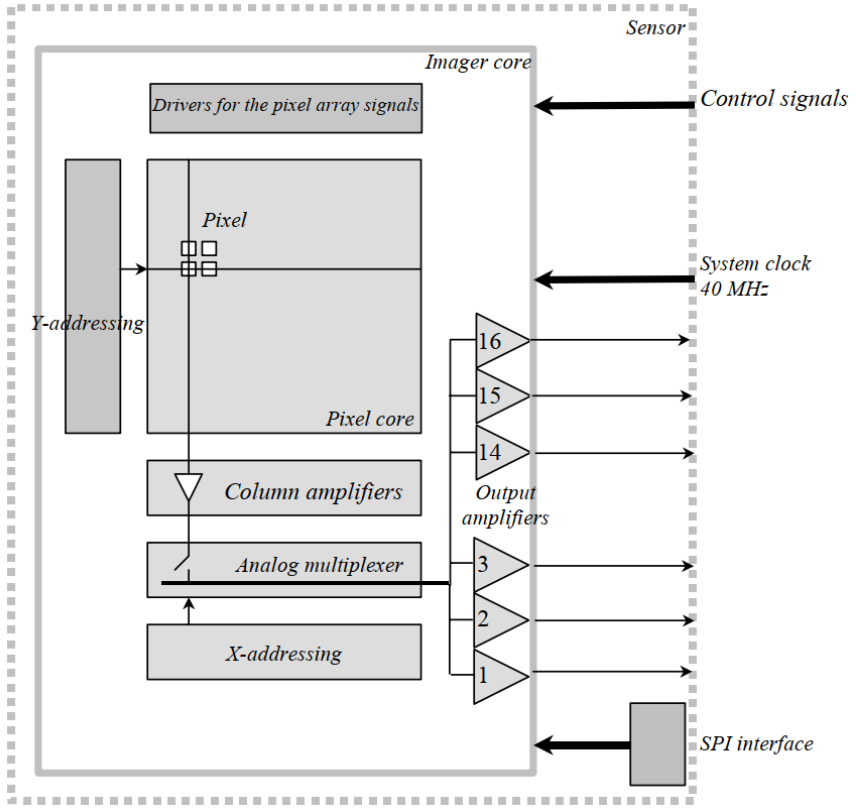

4/ What would be the signal-to-noise ratio (SNR) of an intensity measurement for a single read cycle?

Hint: Let's examine different sources of noise. Even if the ADC had infinite resolution, we would still encounter shot noise and readout noise. Which of these noise sources is the most significant?

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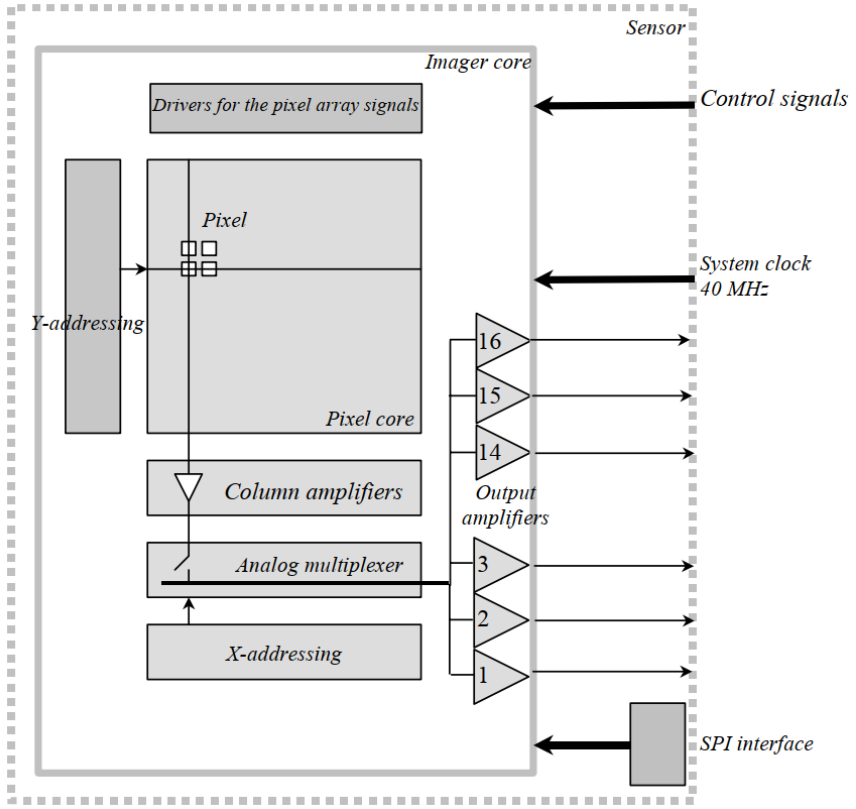

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Hint: Let's examine different sources of noise. Even if the ADC had infinite resolution, we would still encounter shot noise and readout noise. Which of these noise sources is the most significant?

- If there is no signal -> S/N = 0
- When the signal reaches full -> **S = 62500 e^-**. The noise sources are: Shot noise $\sqrt{S} = 250\ e^-$, and dark current/read noise = **45 e^-** . At a first approximation: S/N = 62500/250 = 250. To be more rigorous, we an express the total noise assuming that the noise sources are uncorrelated as:

$$\sigma_{total} = \sqrt{{\sigma_{full\ scale}}^2 + {\sigma_{dark/read}}^2}$$

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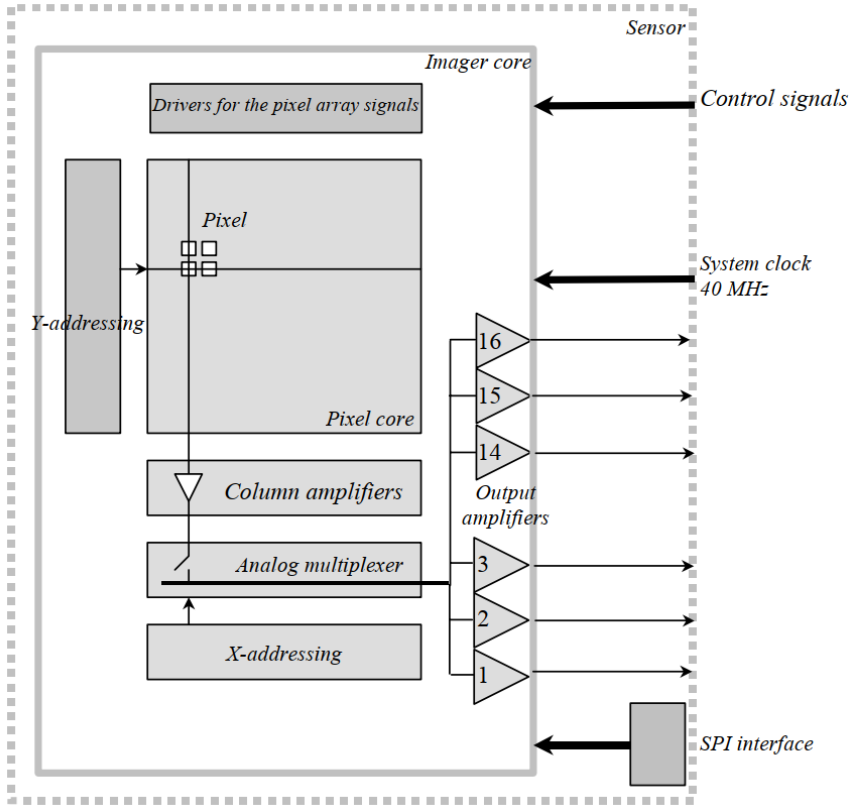

5/ What would be the new SNR value if we average all the data for 1 second?

Reminder: The new standard deviation of the mean can be calculated by dividing the original standard deviation by the square root of the number of measurements averaged (N)

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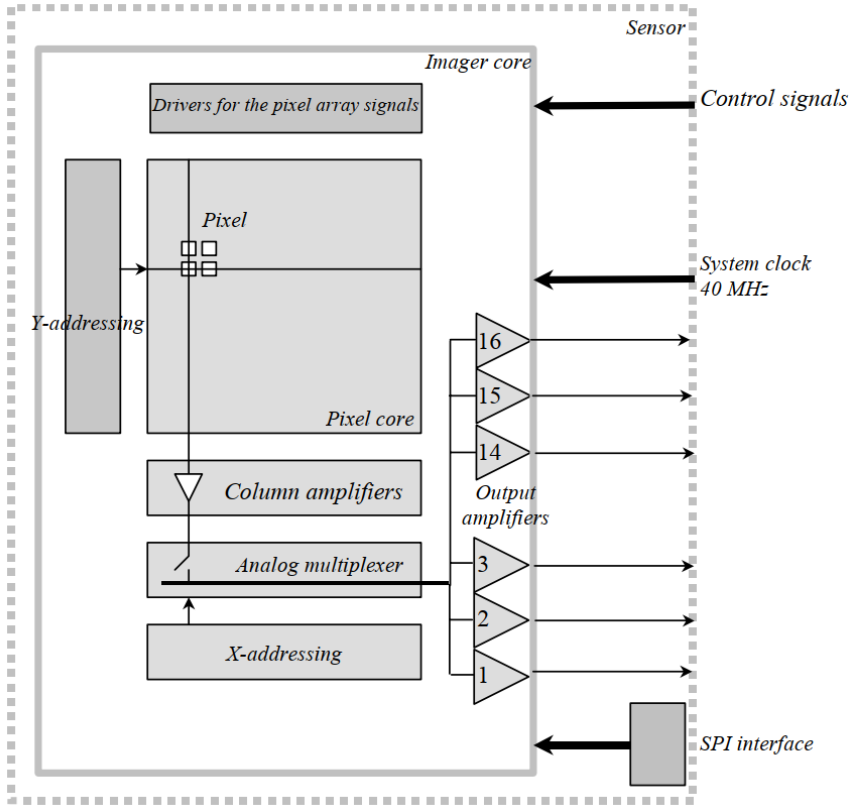

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The uncertainty for a single full-scale read is **250 electrons**, and since there are **488 reads** per second, the uncertainty can be reduced by averaging the measurements. Using the formula for the standard deviation of the mean, the uncertainty of the mean for **488 reads** is reduced to approximately **22 electrons**, which is an **improvement in signal-to-noise ratio by a an order of magnitude compared to a single read.**

Exercise 2: Group explanation

1. Divide yourself in small groups (2-3 ppl).
2. Discuss the following example taken from the lecture, focusing on understanding what is happening.

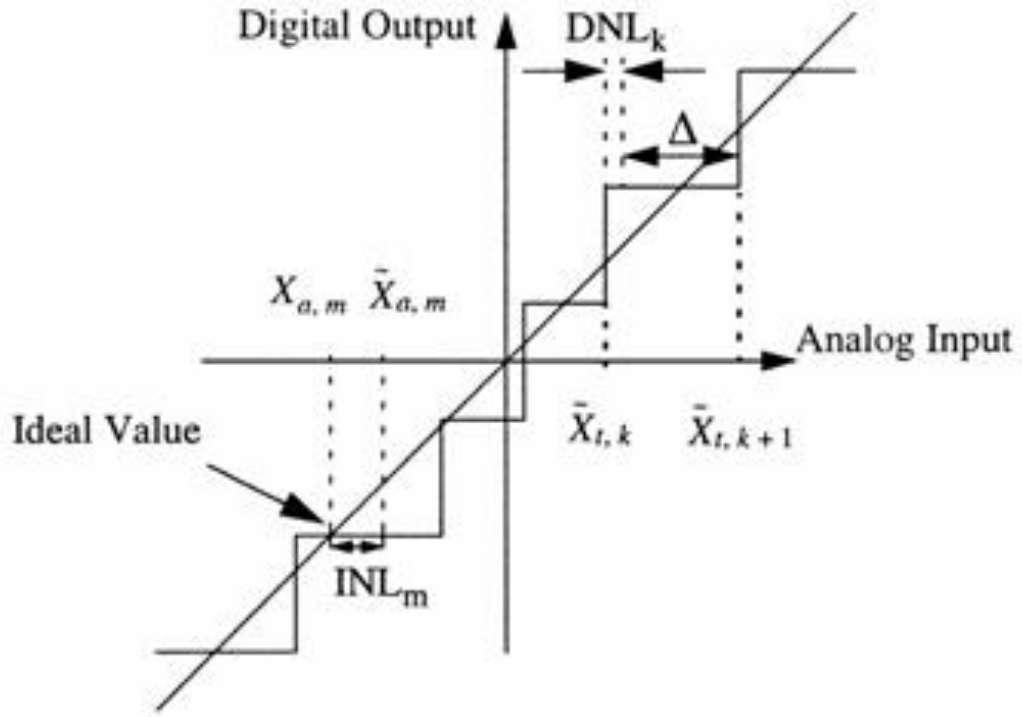
5.2.2 ADC – Real Case

- Non-idealities:
  - Differential non-linearity (DNL)
  - Integral non-linearity (INL)

$$DNL_j \equiv \frac{Width_{ACTUAL,j} - Width_{ID}}{Width_{IDEAL}}$$

$$INL_j = \sum_{k=0}^{k=j} DNL_k$$

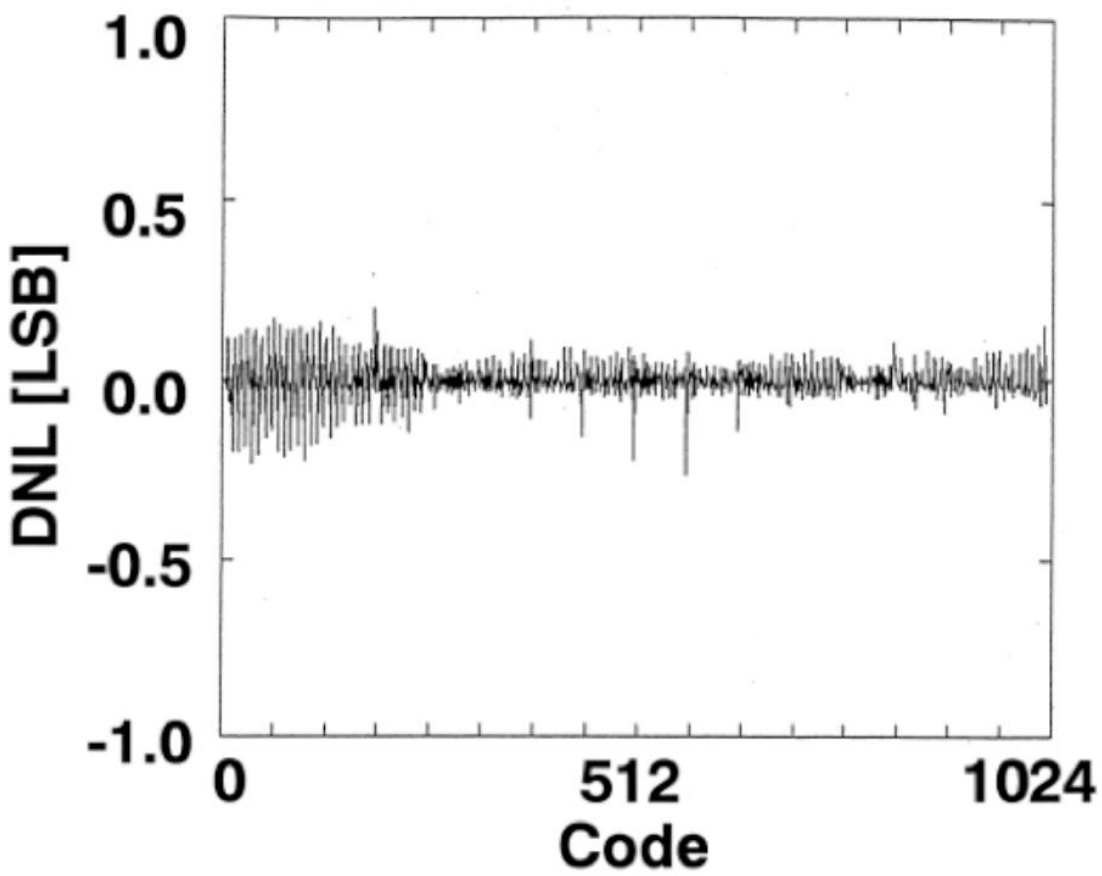
$$DNL_j = INL_{j+1} - INL_j$$

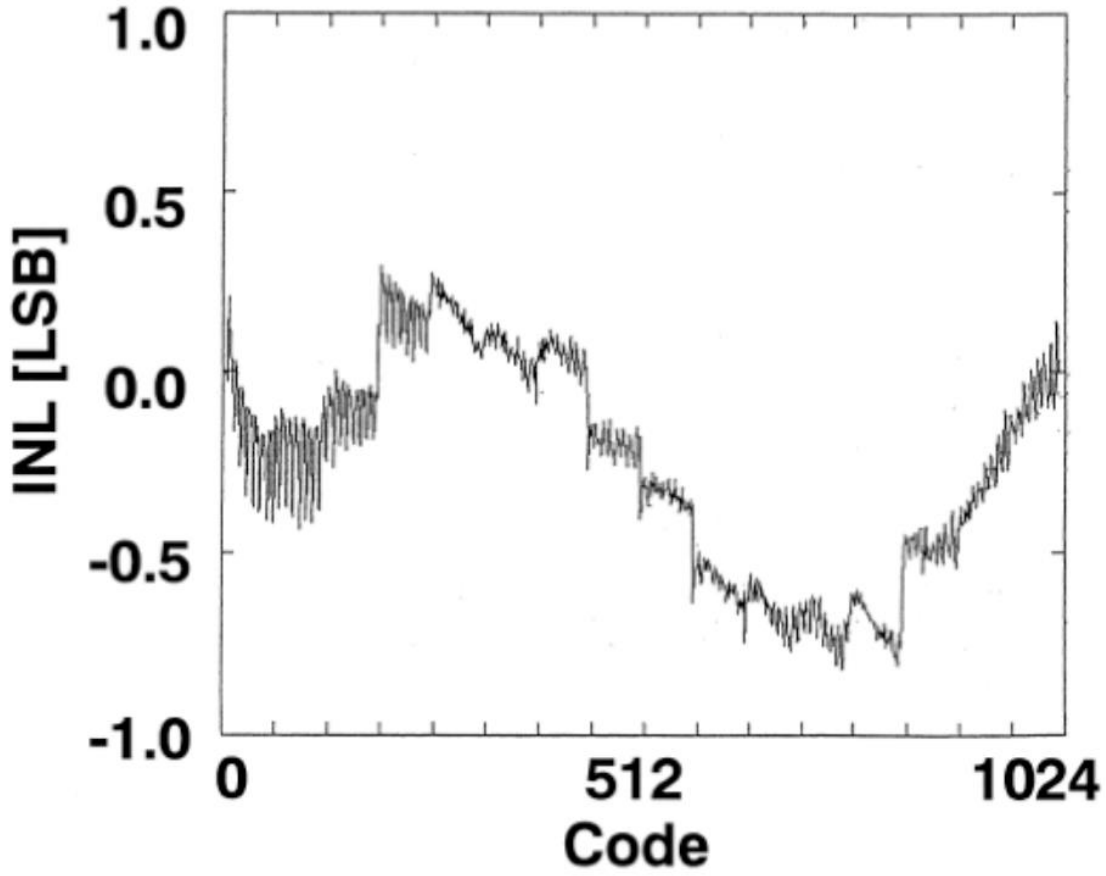


INL = deviation of transfer curve from ideal (linear)

E. Charbon, "Image Sensors – ET 4390 Course Slides", Delft 2016

5.2.2 ADC – Real Case, Example





Source: A. Matzusawa

E. Charbon, “Image Sensors – ET 4390 Course Slides”, Delft 2016

5.2.2 ADC architectures

- Divide yourself in small groups (2-3 ppl).
- Select two ADC architectures and explain them to your colleagues

5.3 TDC architectures

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- Select two TDC architectures and explain them to your colleagues

Exercice 3: Choosing the right architecture

By group of 2-3 pick the right ADC and justify your choice.

Trait / Application	Matching ADC Type
1. Fastest possible conversion speed	
2. Uses a binary search algorithm	
3. Low power, moderate speed, good resolution	
4. Uses an integrator and a counter	
5. Requires one comparator per output level (2^n levels)	
6. Often used in digital multimeters	
7. Uses capacitor array for successive charge balancing	
8. Best suited for audio applications (e.g., microphone)	
9. Has the smallest latency	
10. Balanced in speed, area, and resolution	

Exercice 3: Choosing the right architecture

By group of 2-3 pick the right ADC and justify your choice.

Trait / Application	Matching ADC Type	Justification
1. Fastest possible conversion speed	**Flash ADC**	All comparisons are done in parallel; no iteration, ideal for GHz-speed systems like video or radar.
2. Uses a binary search algorithm	**SAR ADC**	SAR uses a DAC and comparator iteratively to zero in on the input value.
3. Low power, moderate speed, good resolution	**SAR ADC**	Efficient architecture with low switching activity and few analog blocks.
4. Uses an integrator and a counter	**Integrating ADC**	Dual-slope and sigma-delta ADCs integrate input over time before converting.
5. Requires one comparator per output level (2^n levels)	**Flash ADC**	Needs 2^n–1 comparators for n-bit resolution → fast but area and power intensive.
6. Often used in digital multimeters	**Integrating ADC**	High noise immunity and precision over long integration time; ideal for slow, accurate readings.
7. Uses capacitor array for successive charge balancing	**Charge Redistribution ADC**	SAR variant with a binary-weighted capacitor DAC; offers compact design.
8. Best suited for audio applications (e.g., microphone)	**Integrating ADC** (Sigma-Delta)	Sigma-Delta oversampling filters out noise; great linearity and dynamic range for audio.
9. Has the smallest latency	**Flash ADC**	One clock cycle latency — perfect for real-time high-speed applications.
10. Balanced in speed, area, and resolution	**SAR / Charge Redistribution**	SAR (esp. capacitor-based) gives a sweet spot for medium-performance systems (MCUs, sensors).

Exercise 4: Group explanation

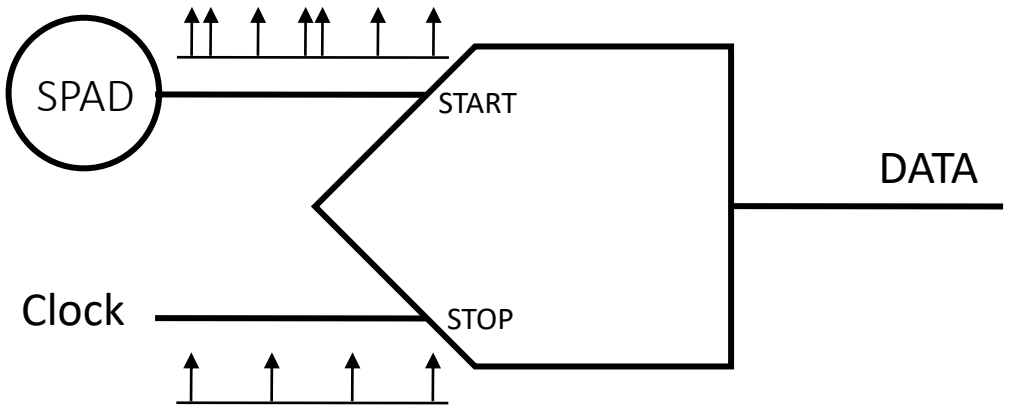
1. Divide yourself in small groups (2-3 ppl).
2. Discuss the following TDC-related Metrology techniques – code-density test and single-shot experiment – focusing on understanding what is happening.

5.3 TDC – Metrology: Optical Tests

A) (Code) Density test: free running SPAD (e.g. natural light source)*

B) Single-shot experiment (e.g. repetitive pulsed laser illumination):

- Histogram Δt_i, i=[1…N] (Time-correlated single-photon counting – TCSPC)



*could also be done electrically

E. Charbon, “Image Sensors – ET 4390 Course Slides”, Delft 2016

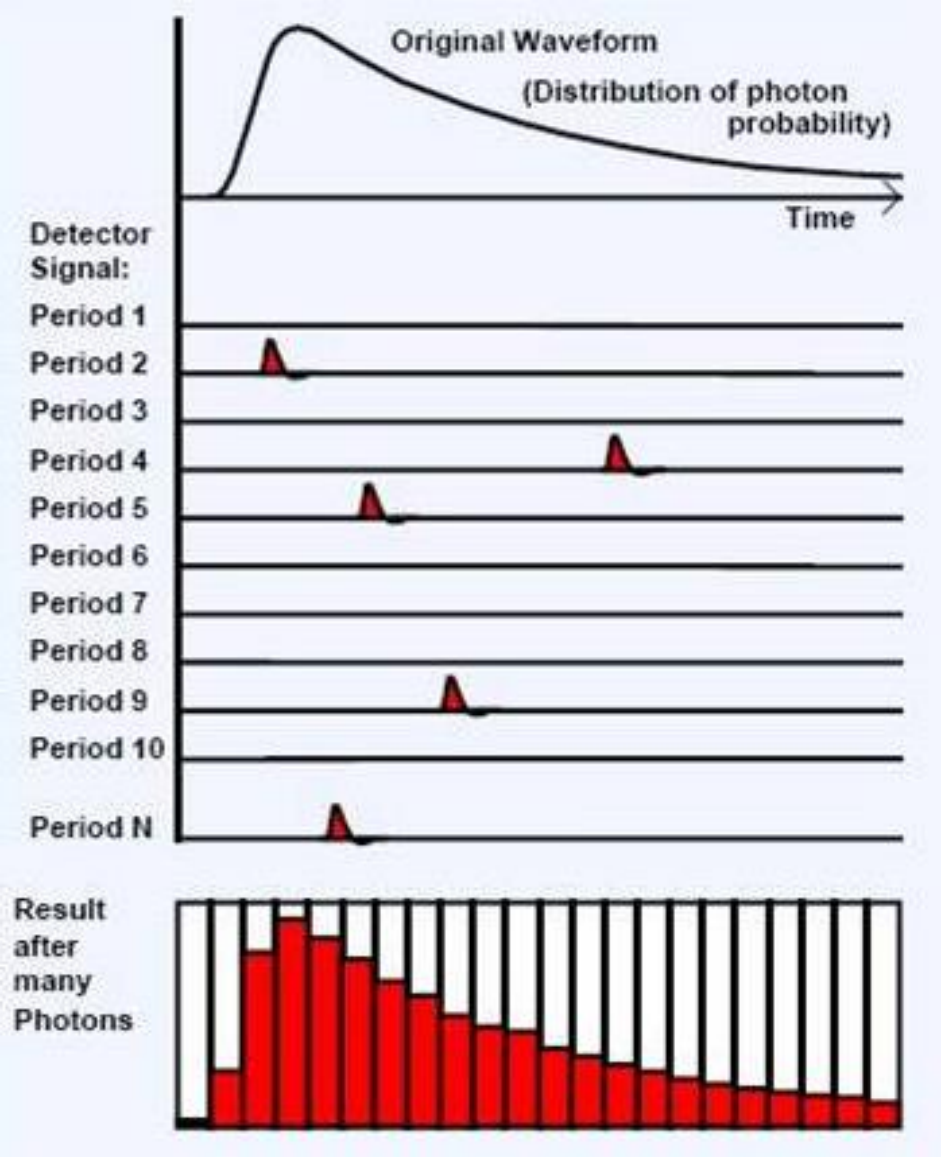
Homework

Homework 1-3 have already been discussed in previous classes and can be relevant to the exam.

Homework 1: Design and analysis of a FLIM System

- Design and analyse a simple Fluorescence Lifetime Imaging (FLIM) system, based on the discussion during the class (TDC application examples, Section 5.3.9):
  a) Estimate the overall system parameters (e.g. fluorophore type, typical process timescales, detector and excitation source). How do their variances add?
  b) Which is the PDF/CDF of the fluorescent sample?
  c) How can you estimate the fluorescence lifetime from i) a timestamp histogram, ii) a series of timestamps?
  d) Which is the standard deviation of the fluorescence lifetime and how does it get better with increasing sample size?
  e) Suppose that there are two fluorophores with different lifetimes (e.g. 2 and 4 ns) and that your measurement system is ideal (negligible measurement error). How many measurements are necessary to differentiate them (rough estimate)?
- *Hint:* Use a Time-Correlated Single-Photon Counting (TCSPC) approach

Homework 1: Reminder: TCSPC Principle



Homework 2: Design and analysis of a LIDAR system

- Design and analyse a simple Light Detection and Ranging (LIDAR) time-of-flight system, based on the discussion during the class (TDC application examples, Section 5.3.9):
  a) Estimate the overall system parameters (target distance, characteristics such as reflectivity, background light, illuminator, detector, time-stamping electronics).

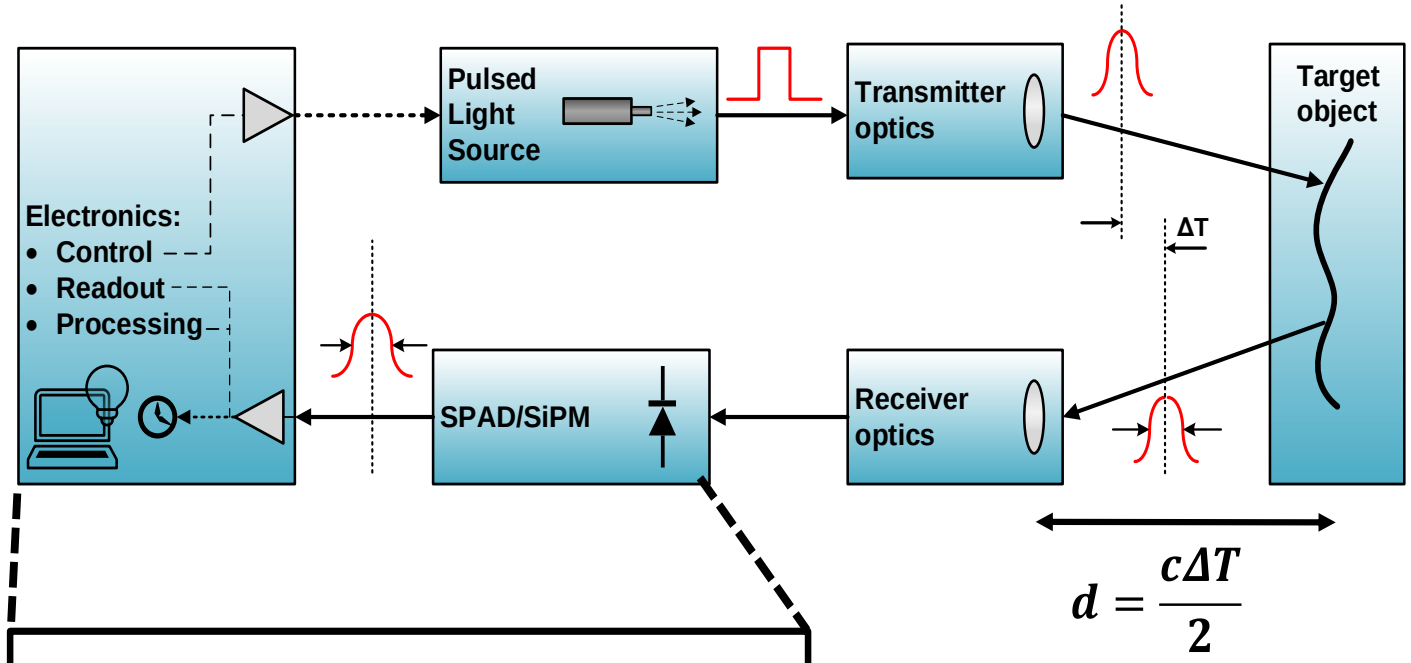
  b) What is the typical PDF of the backscattered light?

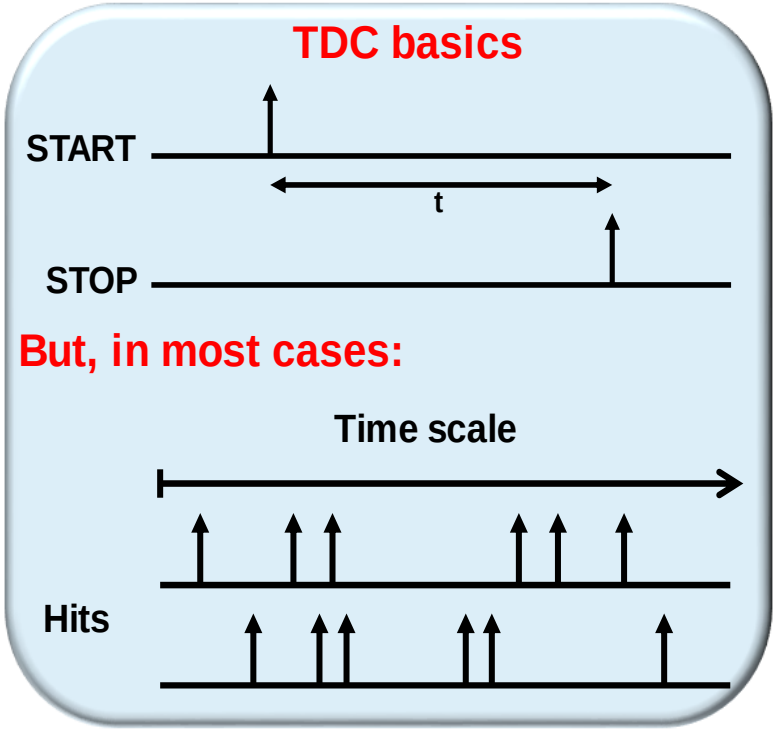
  c) How is it influenced by the precision of the individual components?

  d) How can you increase the measurement precision? And its accuracy?

  e) Suppose that you need to operate at a distance of up to 10 m. Which maximum laser pulse repetition rate can you use?

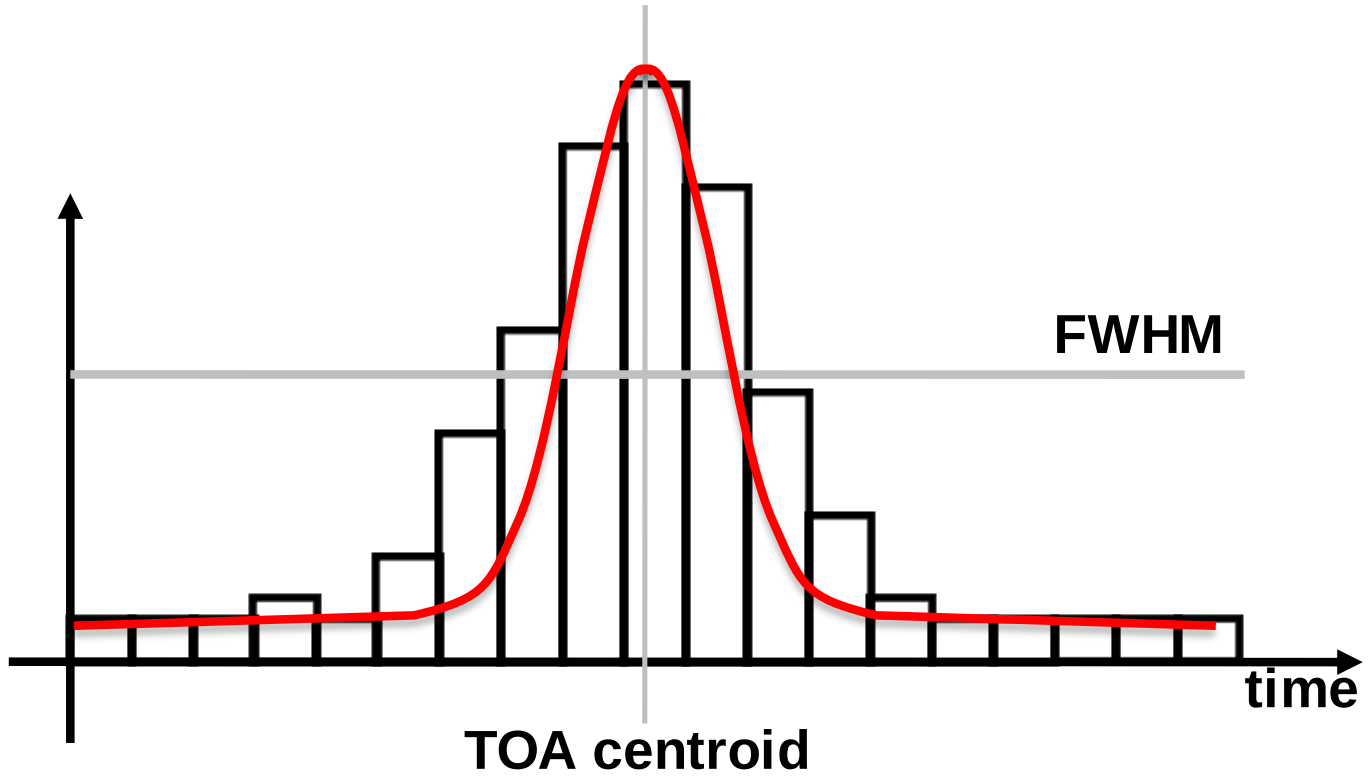
Homework 2: Reminder: 5.3.9 TDC Application Example: Time-of-Flight System





- A chronometer essentially converts time onto a number or a code, like an A/D converter
- Such a converter is known as time-to-digital converter (TDC)

Homework 2: Reminder: 5.3.9 TDC Application Example: Time-of-Flight System



Homework 3: Design and analysis of a PET System

- Design and analyse a simple Positron Emission Tomography (PET) system:
  a) How does the system work (in general terms)?

  b) How does the photodetector module, coupled to a scintillator, work? Which main parameters must be estimated?

  c) Which is the typical PDF of the scintillation light?

  d) How much time does the scintillation light take to travel from the point of impact in the crystal to the photodetector?

  e) Provide some examples of overall time of arrival estimators (estimation theory).

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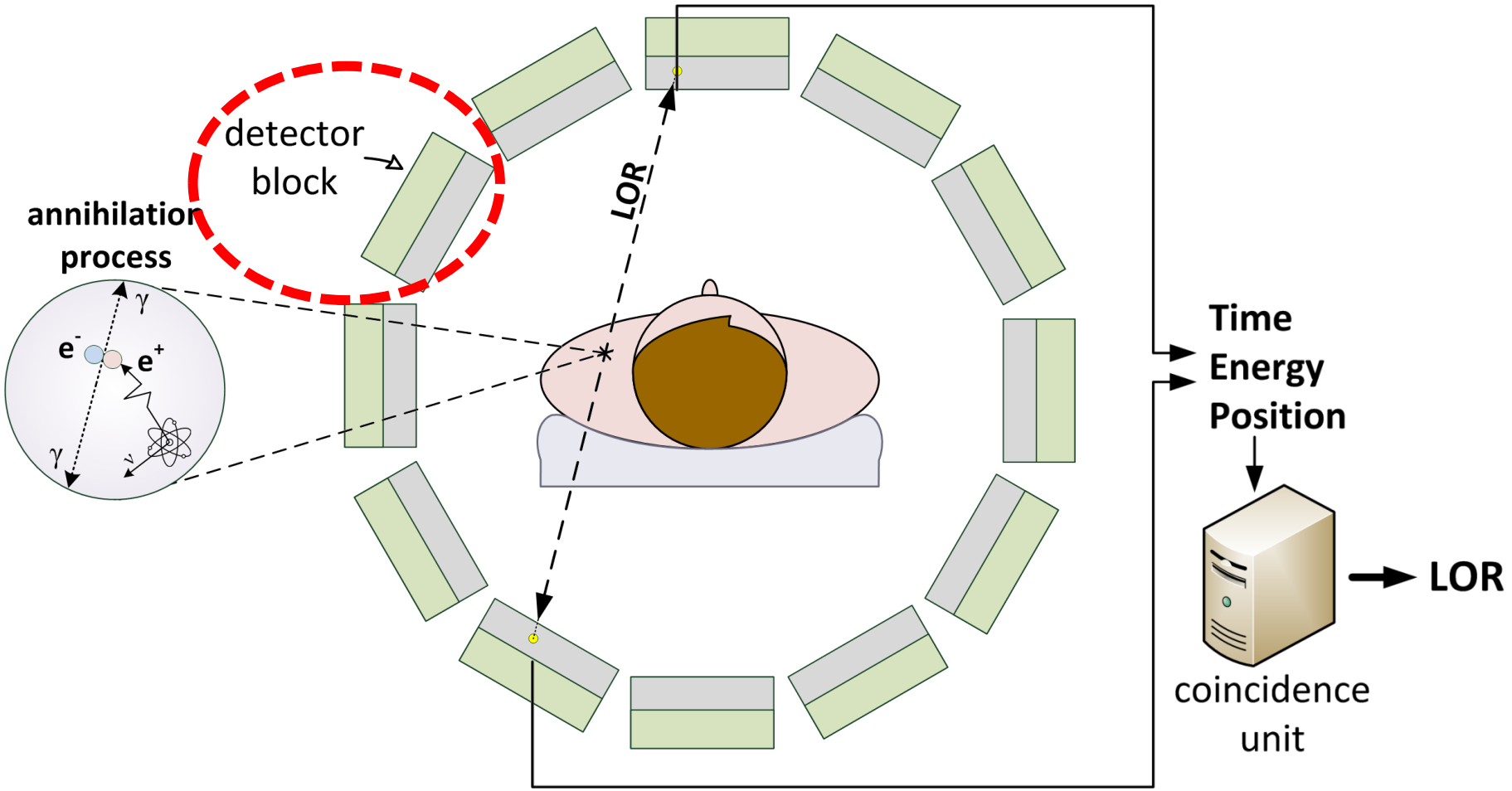

GE Discovery IQ, Nov 2016

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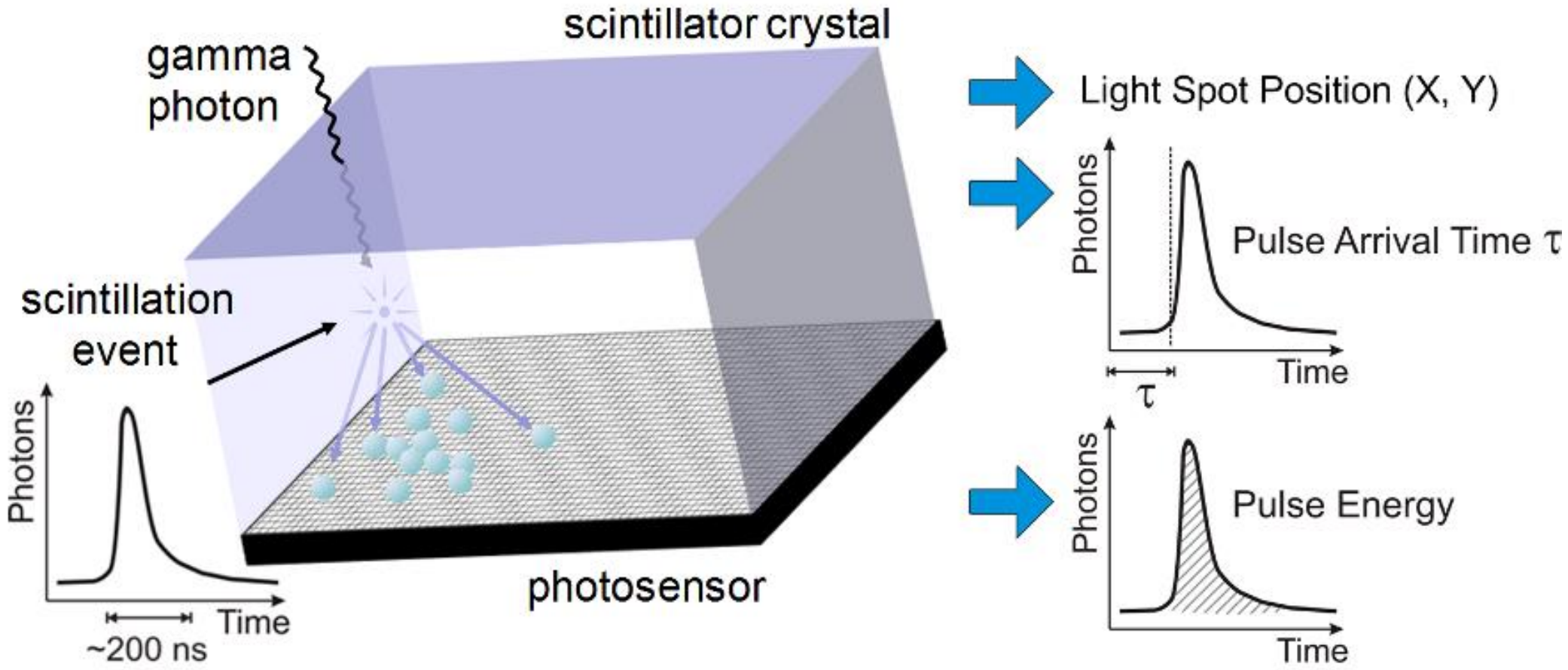


Homework 4: Design case study

Homework 4: Amplifier frequency response (1)

- For any electronic circuit we can derive a transfer function A(s) by small-signal analysis to give

$$A(s) = \frac{N(s)}{D(s)} = \frac{a_0 + a_1 \cdot s + a_2 \cdot s^2 + \cdots + a_m \cdot s^m}{1 + b_1 \cdot s + b_2 \cdot s^2 + \cdots + b_m \cdot s^n}$$

Where $a_0, a_1, \ldots, a_m$ and $b_1, b_2, \ldots, b_n$ are constants.

- Very often the transfer function contains poles only (or the zeros are unimportant). In this case we can factor the denominator to give

$$A(s) = \frac{K}{\left(1 - \frac{s}{p_1}\right)\left(1 - \frac{s}{p_2}\right)\ldots\left(1 - \frac{s}{p_n}\right)}$$

Where K is a constant and $p_1, p_2, \ldots, p_n$ are the poles of the transfer function.

📖 Paul R. Cova, "Analysis and design of analog integrated circuits, 5th edition."

Homework 4: Amplifier frequency response (2)

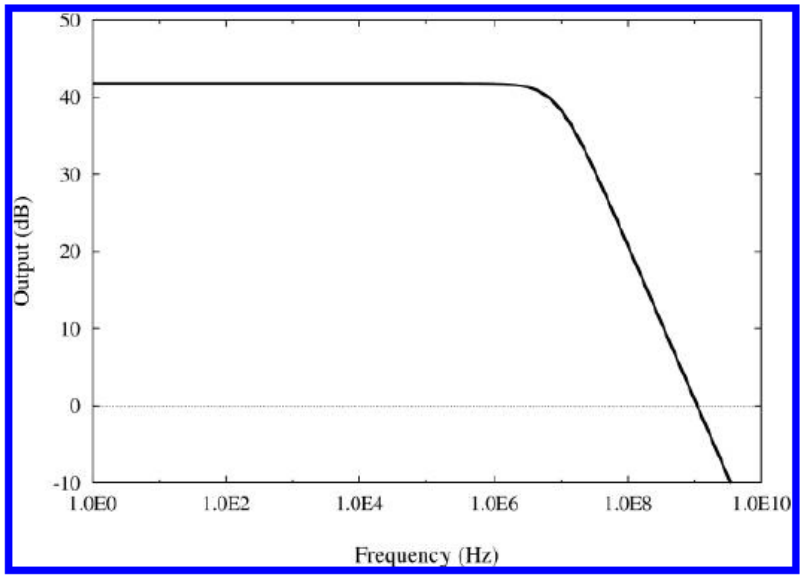
- An important case occurs when one pole is dominant. That is, when $|p_1| \ll |p_2|$, $|p_3|$, …

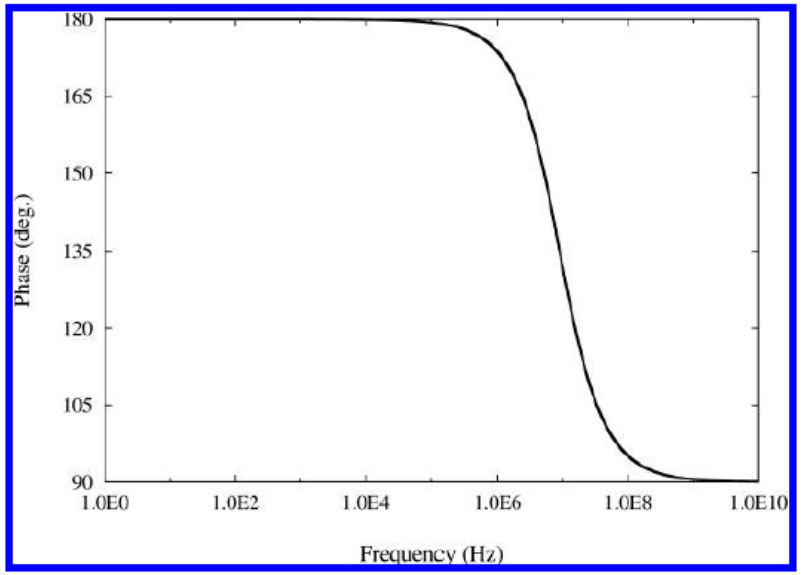
- The gain magnitude in the frequency domain can be approximated as

$$|A(j\omega)| \simeq \frac{K}{\sqrt{1+\left(\frac{\omega}{p_1}\right)^2}}$$

This approximation can accurately predict the -3-dB frequency at least until $\omega \simeq |p_1|$, and we can write

$$\omega_{-3dB} \simeq |p_1|$$



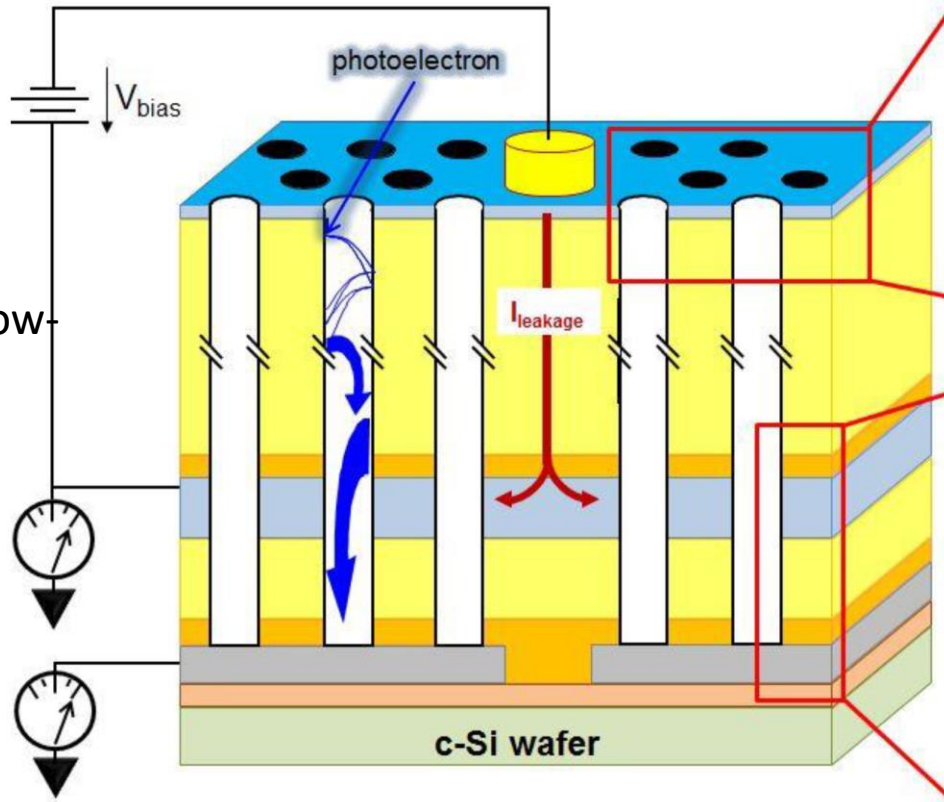


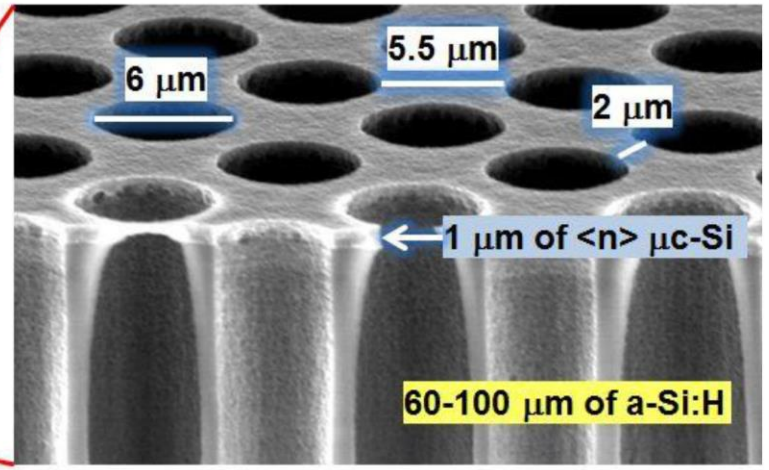
Paul R. Cova, "Analysis and design of analog integrated circuits, 5th edition."

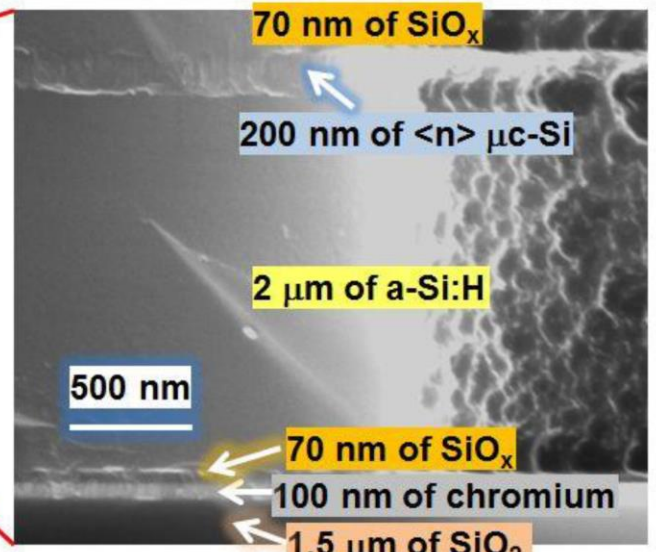
Homework 4: Design case study

Rendering and microscopic (SEM)
view of an a-Si:H based Multi-Channel Plate (aMCP)

Problem: estimate aMCP capacitance to optimize follow-up low noise amplifier



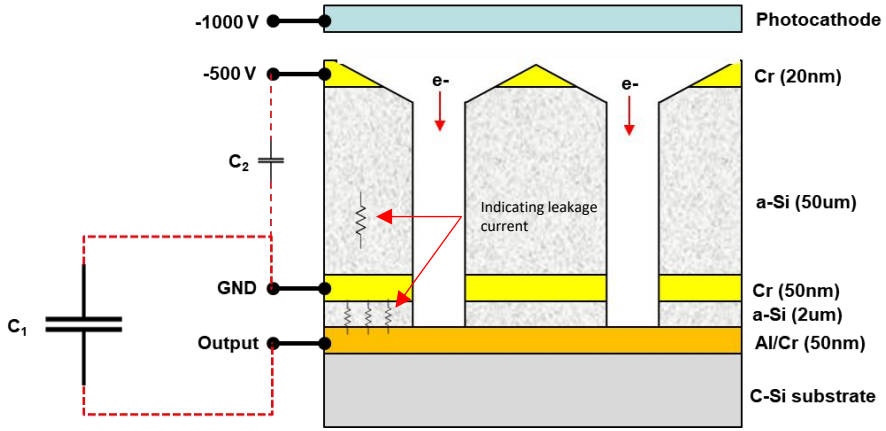




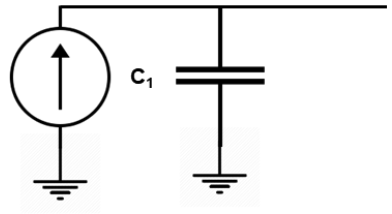
Frey, S., et al. "Characterization of Amorphous Silicon Based Microchannel Plates with High Aspect Ratio." 2019 IEEE NSS/MIC

PV-lab IMT NEUCHATEL

Homework 4 : Design case study



Cross-section view of the aMCP channels



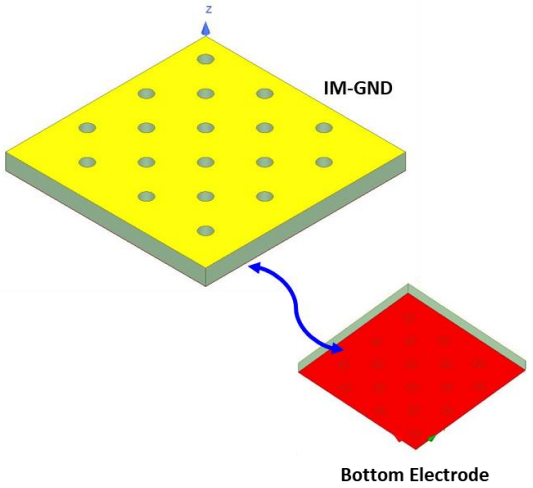
Simplified electrical model of AMCPs

$$C = \varepsilon_r \varepsilon_0 \frac{A}{d}$$

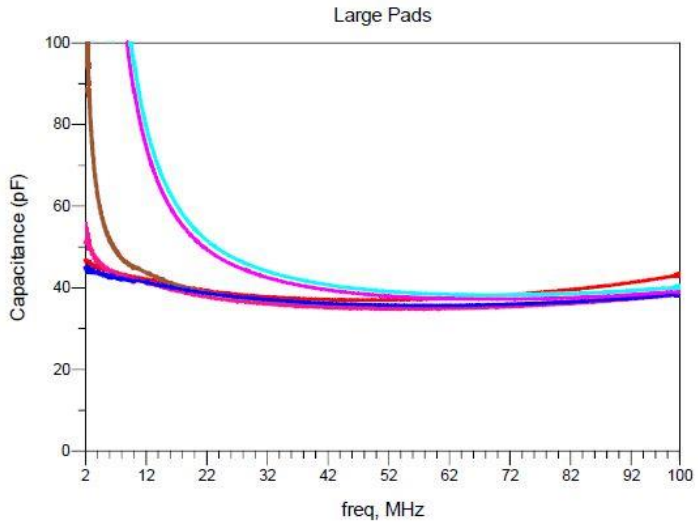
ε_r → ~12 for a-Si:H*

Estimation of AMCP capacitance via parallel plate capacitor (~960 × 960 µm²) → **C_1=~45.5 pF**

vs. ANSYS simulation → **C_1=49.37 pF**



vs. Experimental results (notice a few broken channels)

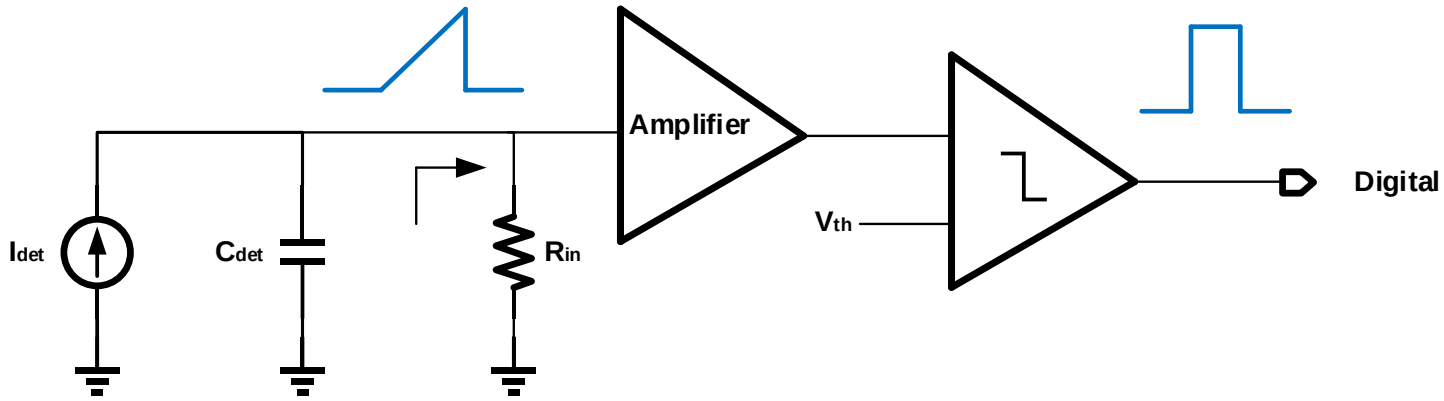


Frey, S., et al. "Characterization of Amorphous Silicon Based Microchannel Plates with High Aspect Ratio." 2019 IEEE NSS/MIC

Homework 4 : Design case study

- Example of detector specifications:

Q_{in} = 3000 e- / 10000 e-
C_{det} = 2 pF
t_{coll} = 10 ps



- *Exercise*: Estimate the pre-amplifier specifications:
  - a/ DC gain
  - b/ -3 dB bandwidth

- *Hint 1:* We always cover the worst case scenario when designing a read-out circuit.
- *Hint 2:* Assume a targeted rise time t_{rise} = 30 ps at the input of the comparator.

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Q_{in} = 3000 e- / 10000 e-
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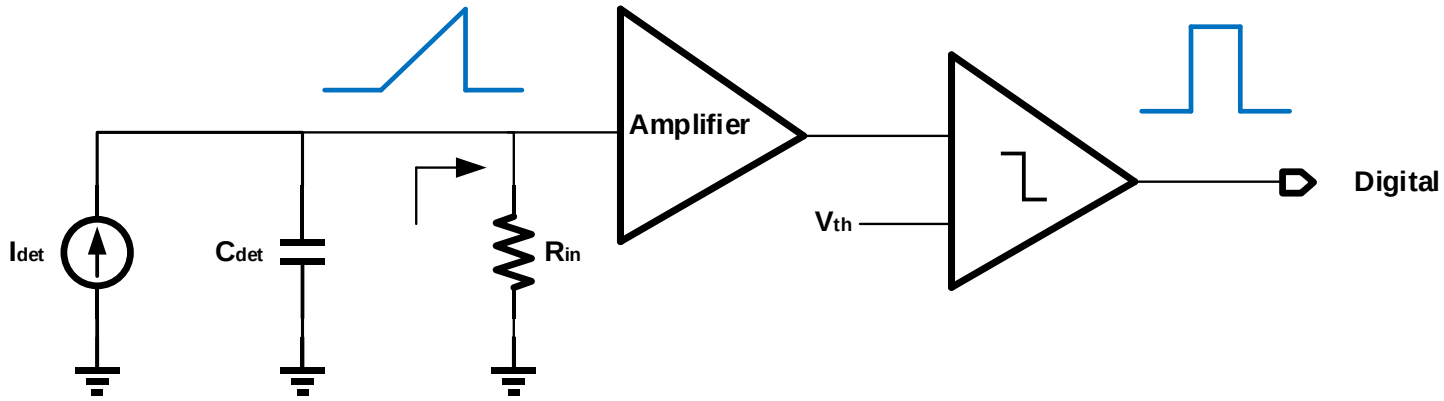

- a/ DC gain

$$V_{in,min} = \frac{Q_{in,min}}{C_{det}} = 0.25 \text{ mV}$$

$$V_{out,min} = 1.5 \cdot V_{th,cmp}$$

$$A_{v,min} = \frac{V_{out,min}}{V_{in,min}} \approx 120$$

$$A_{v,min(dB)} = 20\log(120) \approx \mathbf{42\ dB}$$

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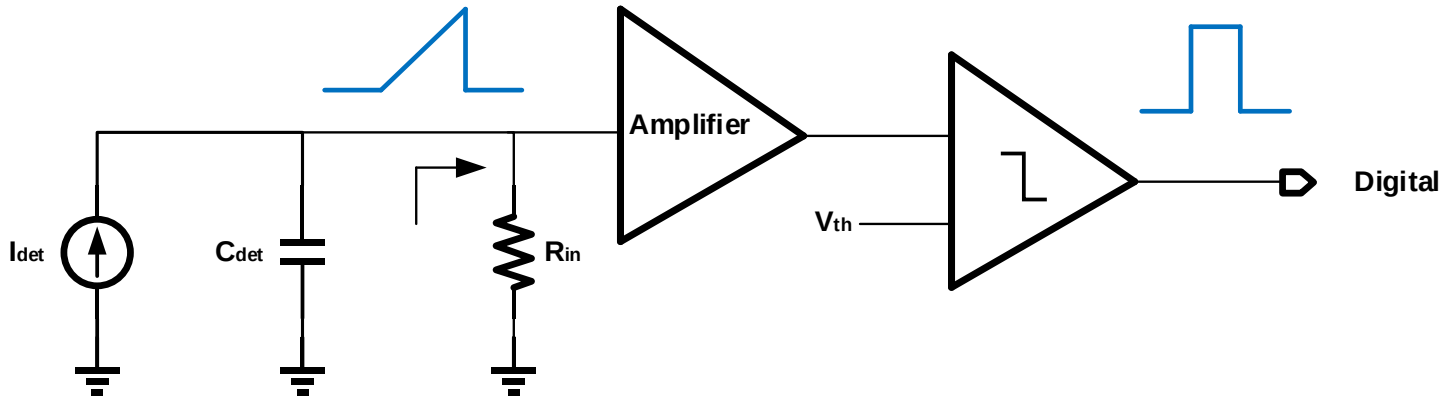


- b/ -3 dB bandwidth

In case the collection time t_{coll} is smaller than the input RC constant, the rise time is higher than the collection time.

- The collected charges are integrated on the detector capacitance.

Homework 4: Design case study

Q_{in} = 3000 e- / 10000 e-
C_{det} = 2 pF
t_{coll} = 10 ps

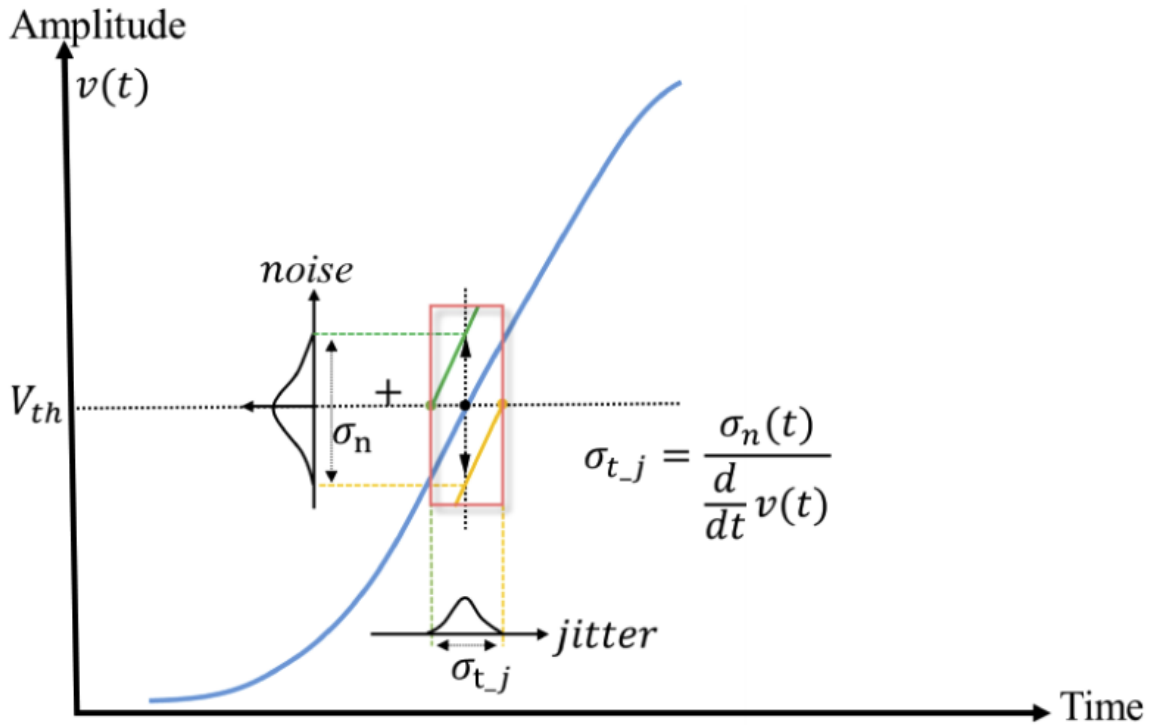
In order to make the comparator less sensitive to noise, the slope at its input should be as steep as possible (ideally $t_{rise} = t_{coll}$).

For our analysis:

t_{rise} = 30 ps

$$f_{-3dB} \approx \frac{0.33}{t_{rise}}$$

→ $f_{-3dB} \approx 11$ GHz



J. Yang, G. Gu, W. Qian, K. Ren, D. Lu, J. Zhang, P. Guo, Q. Gao, M. Wan, and Q. Chen, "Pulsed light time-of-flight measurement based on a differential hysteresis timing discrimination method," Opt. Express 28, 23554-23568 (2020).